**19CSE211-COMPUTER ORGANIZATION AND ARCHITECTURE L-T-P-C: 3-0-3-4**

**Course Objectives**

* This course aims at introducing the concepts of computer architecture and organization.
* It describes overview of MIPS architecture in terms of instruction set, data path and pipelining
* It introduces pipelining and memory systems in detail along with performance metrics for designing computer systems

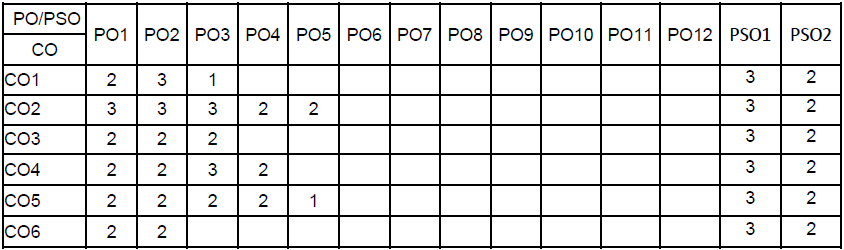
**Course Outcomes**

* **CO1:** Understand the design principles of Instruction Set Architecture (ISA) by taking MIPS as reference.
* **CO2:** Design, and Analyze datapath for instruction execution using Single Clock Cycle
* **CO3:** Understand design of instruction execution using Multiple Clock Cycles and Analyze / Evaluate the

performance of processors.

* **CO4:** Understand Pipelined architecture and Design of 3 and 5 stage pipeline processor in MIPS
* **CO5:** Understand the working of Arithmetic and Logic Unit
* **CO6:** Understanding the concepts of Memory Organization

**CO-PO Mapping**

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**Syllabus**

**Unit 1**

Introduction and Performance of Computing system, Processor Architecture with example as MIPS & Instruction Set, Single Cycle Datapath Design, Control Hardware, Computer Arithmetic, Floating Point Arithmetic, Role of performance.

**Unit 2**

Introduction to multicycle at a path, Pipelining Technique – Design Issues, Hazards: Structural Hazards, Data Hazards and Control Hazards, Static Branch Prediction, Dynamic Branch Prediction, Advanced Concepts in pipelining.

**Unit 3**

Memory Organization - Introduction, Cache Memory Organization, Main Memory & Interleaving, I/O Organization, Modern Processors, Parallel Processing.

**Text Book(s)**

*Patterson DA, Hennessy JL. Computer Organisation and Design, The Hardware/Software interface (ARM Edition). Fourth Edition, Morgan Kaufmann; 2010.*

**Reference(s)**

*Palnitkar S. Verilog HDL: a guide to digital design and synthesis. Second Edition, Pearson Education Asia; 2006.*

*Hamacher et. al. Computer Organisation. Sixth Edition, McGraw-Hill; 2017.*

*Hennessy JL, Patterson DA. Computer architecture: a quantitative approach. Fifth Edition, Morgan Kauffmann; 2011.*

*Hayes JP. Computer Organisation and Architecture. Third Edition, McGraw Hill; 2017.*

*Stallings W. Computer Organisation and Architecture. Tenth Edition, PHI; 2016.*

**Evaluation Pattern**: 65:35